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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/917,312	07/27/2001	Hown Cheng	Stream-09US	9556

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LAW OFFICES OF IMAM
111 N. MARKET STREET, SUITE 1010
SAN JOSE, CA 95113

EXAMINER	
COLEMAN, ERIC	
ART UNIT	**PAPER NUMBER**
2183	

DATE MAILED: 07/27/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/917,312	CHENG ET AL.	
	Examiner	Art Unit	
	Eric Coleman	2183	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 May 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *27-47* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *27-47* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. Claims 27-29, 31-33, 41-43,45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozcelik (patent No. 5,928,321) and Bublil (patent No. 6,012,137) in view of Chen (patent No. 6,473,864) and Mohamed et al. (patent No. 5,978,838).

2. Ozcelik taught invention substantially as claimed including a data processing ("DP") system comprising:

a) Processing unit RISC CPU 100) (e.g., see fig. 1 and col. 5, lines 41-54);

b) Instruction cache (104,150) coupled to the processing unit;

c) Code random access memory (102) coupled to the processing unit;

d) Data memory (112) and another data memory (152) (e.g., see col. 8, lines 23-31) coupled to the processing unit;

e) Register group (132,134 and another register group 138,140))(e.g., see fig. 1). Ozcelik did not expressly detail (claim1) the code random access memory storing instructions required for causing serving of time critical-tasks and the cache for storing instructions of non-time critical tasks. Chen however taught separately storing time in a code ram (SRAM 104) instructions for serving time critical tasks (e.g., see fig.3, and col. 2, line 36-col. 3, line 15), and storing non-time critical code in a second memory (e.g., see col. 2, lines 23-35). The Ozcelik instruction memory and code ram were both external to the microprocessor. It was well known in the art to provide an on-chip cache (i.e., L1 cache) in conventional microprocessors to facilitate retrieval of instructions for

execution. Therefore one of ordinary skill would have been motivated to provide an on chip cache to facilitate transfer of data from the off chip slow program memory at least to facilitate quick retrieval of program instructions stored in the slow program memory for execution.

3. Ozcelik did not expressly detail (claim 27,41) that the register groups comprised one for updating the status of registers related to time critical tasks and another register group. Mohamed taught a system with the register groups that comprised a register group (243,244) for access by time critical tasks (multimedia tasks) and a register group (272) for access by non-time critical tasks (control tasks). (e.g., see fig. 2 and col. 4, line 21-col. 4, line 63). Therefore in the processing of tasks the register groups would have respectively updated status of registers related to time-critical task and non-time critical tasks.

4. It would have been obvious to one of ordinary skill in the DP art at the time of the claimed invention to combine the teachings of Ozcelik and Chen. Both references were directed toward the problems of processing time-critical tasks in a DP system. The addition of the Chen teachings of separately storing the time critical instructions and non-time-critical instruction would allow the system to separately access time instructions for critical and non-time critical tasks by storing time off chip time critical tasks on a fast memory and non-time critical tasks on a slower memory to reduce system cost which efficiently access both time critical and non-time-critical tasks.

5. It would have been obvious to one of ordinary skill in the DP art at the time of the claimed invention to combine the teachings of Ozcelik and Mohamed. Both references

were directed toward the problems of processing time-critical tasks in a DP system. The addition of the Mohamed teachings of separate registers for time critical task and non-time critical task would have enabled the combined system to separately access time critical task data and non-time critical tasks data efficiently so that tasks would not have to wait for access to stored data.

6. Claim 27 comprises the limitation of wherein the processing unit need access status of registers only in the register group for execution of time-critical tasks thereby avoiding saving and restoring status of another registers for execution of time-critical tasks. As to this limitation Mohamed taught separate register groups or files for time critical and non-time critical tasks (e.g., see fig.2) wherein the means for processing time critical tasks cannot access the registers for non-time ciritical control tasks (e.g, see col. 6, lines 37-67). Mohmaed also taught the time critical task saves its status while the non-critical task waits for the critical task to become idle (e.g., see col. 7, lines 7-53). Therefore with the separation of the time critical registers and non-time critical task registers, when processing time critical tasks only the time critical task (multimedia) registers for time critical task would have needed to be accessed, and therefore only the status of those registers would have needed to be accessed (e.g., see figs.1,2 and col. 6, lines 20-62).

7. As per claims 31,45, Bublil taught the demultiplexing of video and audio data (e.g., see fig. 1) Audio/ Video data organized to the MPEG standard was well known in the art at the time of the claimed invention. Therefore one of ordinary skill in the art

would have been motivated to use MPEG data for the demultiplexing to coherently communicate with other systems that communicate using MPEG standard.

8. As to claims 32,46, Bublil taught sending video data to a monitor via line 130 in figure 1. User interface applications such as receiving input from the user were well known in the art at the time of the claimed invention to not be time critical as the internally clocked operations of processing that inherently require to be processed in a much shorter time period than the processing of the user interface.

9. As to claims 28,42, Bublil taught delivery of video information to output encoder 108 for output to monitor (e.g., see fig. 1). As discussed above the providing of additional data for video streaming would have required to be performed in a time-critical manner requiring a high priority to provide the encoded or compressed video data to the monitor via the line 130 in Bublil. Otherwise the video shown on the screen would not be updated in time to provide a seamless video.

10. As to claims 29,33,43,47, Ozcelik and Bublil taught a system that provided video data to a monitor via line 130 in figure 1 of Bublil. Therefore in the performance of off the shelf applications there would have been a requirement to send additional data to the monitor screen to update the screen. The video data for streaming video clearly would have required sending additional data for fast update of the screen within the range of microseconds. In the other applications such a pop-up screens for advertising and word processing applications when the processor is busy processing many applications simultaneously the update of the screen would have occurred less frequently namely in the range of seconds. The operator normally can only key in data

at a few characters per second. However when the processor is processing many applications simultaneously it was well known in the art for the user to wait for the processor to wait for the processor to update the screen with characters in the range of seconds. With this limitation sending data to the screen during video comprise or encoding would have been in the range of microseconds and the number of microseconds selected clearly would have been system dependent and the interval under two microseconds would have been recognized by one of ordinary skill to be part of at least one implementation of the Ozcelik and Bublil teachings. Also one of ordinary skill would have recognized that in at least one implementation of the Ozcelik and Bublil teachings the screen would have been updated for certain applications such as pop-up window advertisement and word processing in every two seconds.

11. Claims 30,44,are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozcelik and Bublil in view of Chen and Mohamed as applied to claim 27 above, and further in view of Kiryama (patent No. 5,561,466).

12. Kiryama taught multiplexing of audio and video streams (e.g., see figs. 1,5 and col. 4, lines 27-53).

13. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Ozcelik and Kiryama. Both references comprise the encoding of video and audio data. Ozcelik taught demultiplexing and multiplexed of video and audio data. The incorporation of the Kiryama teachings of multiplexing of the demultiplexed video and audio data would have provided for efficient transmission of data on one transmission medium.

14. Claims 34-40 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozcelik (patent No. 5,928,321) and Bublil (patent No. 6,012,137) in view of Chen (patent No. 6,473,864) and Mohamed (patent No. 5,978,838) and Young (patent No, (patent No. 5,619,706).

15. Ozcelik taught invention substantially as claimed including a data processing ("DP") system comprising:

a) Processing unit RISC CPU 100) (e.g., see fig. 1 and col. 5, lines 41-54);

b) Instruction cache (104,150) coupled to the processing unit;

c) Code random access memory (102) coupled to the processing unit;

d) Data memory (112) and another data memory (152) (e.g., see col. 8, lines 23-31) coupled to the processing unit;

e) Register group (132,134 and another register group 138,140))(e.g., see fig. 1). Ozcelik did not expressly detail (claim1) the code random access memory storing instructions required for causing serving of time critical-tasks and the cache for storing instructions of non-time critical tasks. Chen however taught separately storing time in a code ram (SRAM 104) instructions for serving time critical tasks (e.g., see fig.3, and col. 2, line 36-col. 3, line 15), and storing non-time critical code in a second memory (e.g., see col. 2, lines 23-35). The Ozcelik instruction memory and code ram were both external to the microprocessor. It was well known in the art to provide an on-chip cache (i.e., L1 cache) in conventional microprocessors to facilitate retrieval of instructions for execution. Therefore one of ordinary skill would have been motivated to provide an on chip cache to facilitate transfer of data from the off chip slow program memory at least

to facilitate quick retrieval of program instructions stored in the slow program memory for execution.

16. Ozcelik expressly detailed that the teachings of Bublil (Serial Number 08/865749 now patent No. 6012,137) were expressly incorporated by reference (e.g., see col. 1, lines 33-47).

17. Ozcelik did not expressly detail (claim 34) that the register groups comprised one for updating the status of registers related to time critical tasks and another register group. Mohamed taught a system with the register groups that comprised a register group (243,244) for access by time critical tasks (multimedia tasks) and a register group (272) for access by non-time critical tasks (control tasks). (e.g., see fig. 2 and col. 4, line 21-col. 4, line 63). Therefore in the processing of tasks the register groups would have respectively updated status of registers related to time-critical task and non-time critical tasks.

18.

19. It would have been obvious to one of ordinary skill in the DP art at the time of the claimed invention to combine the teachings of Ozcelik and Chen. Both references were directed toward the problems of processing time-critical tasks in a DP system. The addition of the Chen teachings of separately storing the time critical instructions and non-time-critical instruction would allow the system to separately access time instructions for critical and non-time critical tasks by storing time off chip time critical tasks on a fast memory and non-time critical tasks on a slower memory to reduce system cost which efficiently access both time critical and non-time-critical tasks.

20. It would have been obvious to one of ordinary skill in the DP art at the time of the claimed invention to combine the teachings of Ozcelik and Mohamed. Both references were directed toward the problems of processing time-critical tasks in a DP system. The addition of the Mohamed teachings of separate registers for time critical task and non-time critical task would have enabled the combined system to separately access time critical task data and non-time critical tasks data efficiently so that tasks would not have to wait for access to stored data.

21. Ozcelik did not expressly detail (claims 34) a high priority interrupt controller and low priority interrupt controller coupled to the processing unit. Bublil taught an interrupt controller (208) for controlling interrupts (e.g., see fig. 2a and col. 17, lines 4-16). Ozcelik expressly detailed that the teachings of Bublil (Serial Number 08/865749 now patent No. 6012,137) were expressly incorporated by reference (e.g., see col. 1, lines 33-47).

22. Ozcelik taught storing code for interrupt service routines for time-critical tasks that are commenced immediately and not stalled in a permanent portion of instruction memory (e.g., see col. 3, lines 33-36 and col. 4, lines 21-56 and col. 6, lines 17-31) and storing lower priority of non-time critical routines in a off-chip memory and swapping the instructions into permanent memory with the instructions are to be executed (e.g., see col. 4 ,lines 28-42) where lower priority routines include relatively straightforward interrupt routines (e.g., see col. 9, lines 25-49). Consequently, one of ordinary skill would have been motivated to incorporate interrupt service controllers for the time

critical tasks and non-time critical tasks to provide separate scheduling of the high priority time critical task and the low priority non-time critical tasks. This would provide for efficient control of prioritizing service routines into permanent memory especially while time critical interrupt was being processed by a high priority interrupt controller (e.g., see col. 12, lines 5-64).

23. On the other hand Young taught the use of plural independent interrupt controllers for separate groups of interrupts (e.g., see col. 3 lines 20-43).

24. It would have been obvious to one of ordinary skill to combine the teachings of Ozcelik and Young. Both references were directed toward the problems of processing plurality of groups of interrupts in a processing system. The incorporation of the Young teachings of plural interrupt controllers would have provided separate and more efficient control and scheduling of different groups of interrupts for the combined system.

25. As to the dedicating of the cache, register group data memory and low-priority interrupt controller for low priority tasks, Ozcelik separates the storage of the low priority and the high priority instructions in a RISC system. The DRAM acts as a low level cache memory that stores the low priority instructions along with the registers that would be used in a register windowing RISC system that separately stores data for different routines in a different set of registers as well as the DRAM that stores data for processing the low priority. Also the High priority instructions are stored in the permanent memory while data memory 112 is used for high priority interrupt routines and in the register windowing RISC each routine has its own group of registers. The dedicating of separate interrupt controllers in the Ozcelik system was discussed above.

26. As to claim 35, Bublil taught delivery of video information to output encoder 108 for output to monitor (e.g., see fig. 1). As discussed above the providing of additional data for video streaming would have required to be performed in a time-criticl manner requiring a high priority to provide the encoded or compressed video data to the monitor via the line 130 in Bublil. Otherwise the video shown on the screen would not be updated in time to provide a seamless video.

27. As to claims 36,40, Ozcelik and Bublil taught a system that provided video data to a monitor via line 130 in figure 1 of Bublil. Therefore in the performance of off the shelf applications there would have been a requirement to send additional data to the monitor screen to update the screen. The video data for streaming video clearly would have required sending additional data for fast update of the screen within the range of microseconds. In the other applications such a pop-up screens for advertising and word processing applications when the processor is busy processing many applications simultaneously the update of the screen would have occurred less frequently namely in the range of seconds. The operator normally can only key in data at a few characters per second. However when the processor is processing many applications simultaneously it was well known in the art for the user to wait for the processor to wait for the processor to update the screen with characters in the range of seconds. With this limitation sending data to the screen during video comprise or encoding would have been in the range of microseconds and the number of microseconds selected clearly would have been system dependent and the interval under two microseconds would have been recognized by one of ordinary skill to be part of at least one implementation

of the Ozcelik and Bublil teachings. Also one of ordinary skill would have recognized that in at least one implementation of the Ozcelik and Bublil teachings the screen would have been updated for certain applications such as pop-up window advertisement and word processing in every two seconds.

28. As per claims 38, Bublil taught the demultiplexing of video and audio data (e.g., see fig. 1) Audio/ Video data organized to the MPEG standard was well known in the art at the time of the claimed invention. Therefore one of ordinary skill in the art would have been motivated to use MPEG data for the demultiplexing to coherently communicate with other systems that communicate using MPEG standard.

29. As to claims 39, Bublil taught sending video data to a monitor via line 130 in figure 1. User interface applications such as receiving input from the user were well known in the art at the time of the claimed invention to not be time critical as the internally clocked operations of processing that inherently require to be processed in a much shorter time period than the processing of the user interface.

30. Claims 37,are rejected under 35 U.S.C. 103(a) as being unpatentable over Ozcelik and Bublil in view of Chen and Mohamed and Young as applied to claim 34 above, and further in view of Kiryama (patent No. 5,561,466).

31. Kiryama taught multiplexing of audio and video streams (e.g., see figs. 1,5 and col. 4, lines 27-53).

32. It would have been obvious to one of ordinary skill in the DP art to combine the teachings of Ozcelik and Kiryama. Both references comprise the encoding of video and audio data. Ozcelik taught demultiplexing and multiplexed of video and audio data. The

incorporation of the Kiryama teachings of multiplexing of the demultiplexed video and audio data would have provided for efficient transmission of data on one transmission medium.

Response to Arguments

Applicant's arguments with respect to claims 27-47 have been considered but are moot in view of the new ground(s) of rejection.

Divine (patent No. 6,081,783) disclosed a dual processor digital audio decoder (e.g., see abstract).

Yoshioka (patent No. 6,310,921) disclosed a Media processing apparatus (e.g., see abstract).

Baron (patent No. 5,586,293) disclosed a rea-time cache implemented by on-chip memory (e.g., see abstract).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric Coleman whose telephone number is (571) 272-4163. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Chan can be reached on (571) 272-4162. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

EC

ERIC COLEMAN
PRIMARY EXAMINER